Flip Flops
(JK Flip Flop)

Presented By:

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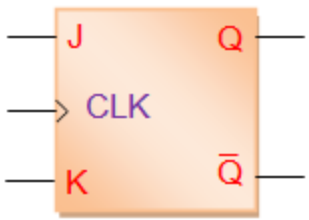
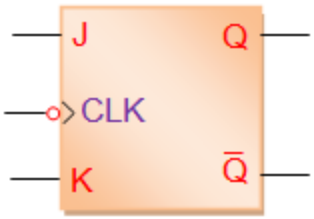
JK Flip Flop

JK Flip-Flop

A **JK flip-flop** is a sequential bi-state single-bit memory device named after its inventor by **Jack Kil**. In general it has one clock input pin (CLK), two data input pins (J and K), and two output pins (Q and $\overline{Q}$) as shown in Figure. JK flip-flop can either be triggered upon the leading-edge of the clock or on its trailing edge and hence can either be (a) positive - or (b) negative- edge-triggered, respectively.



(a)



(b)

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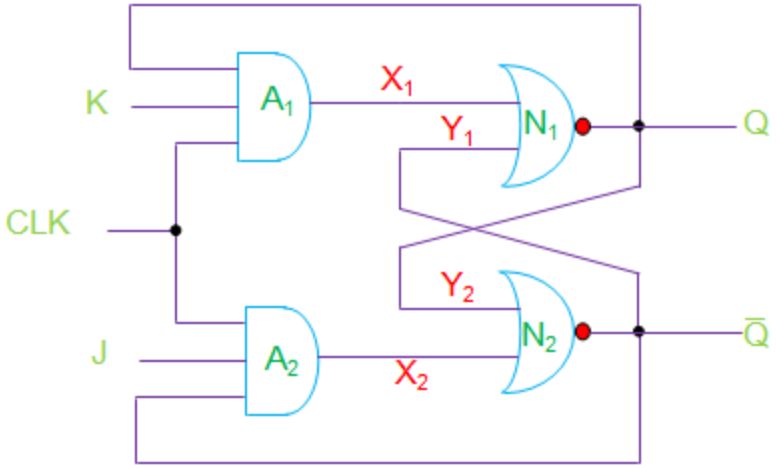
In order to have an insight over the working of JK flip-flop, it has to be realized in terms of basic gates similar to that in Figure which expresses a positive-edge triggered **JK flip-flop** using AND gates and NOR gates.



Here it is seen that the output Q is logically *anded* with input K and the clock pulse (using AND gate 1, A_1) while the output $\overline{Q}$ is *anded* with the input J and the clock pulse (using AND gate 2, A_2).

Further the output of A_1 is fed as one of the inputs (X_1) to the NOR gate 1, N_1 whose other input (Y_1) is connected to output $\overline{Q}$. Similarly NOR gate 2, N2 has its two inputs (X2 and Y2) as the output of A_2 and output Q (respectively).

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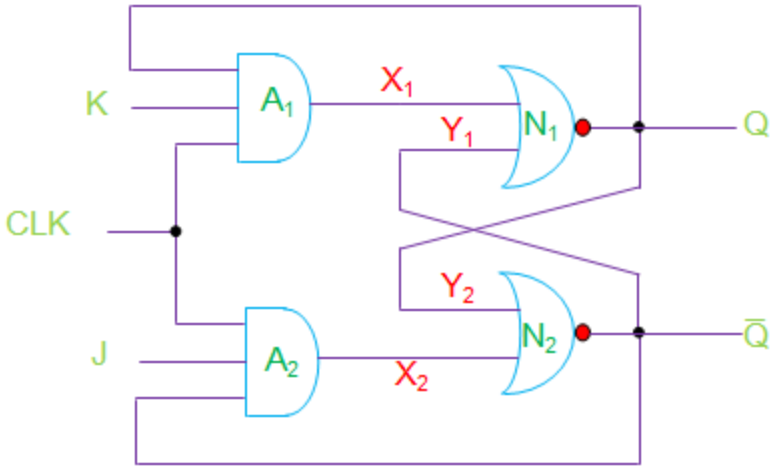
Initially let J = K = 0, Q = 0 and $\overline{Q}$ = 1. Now consider the appearance of positive-edge of the first clock pulse at the CLK pin of the flip-flop. This results in $X_1 = 0$ and $X_2 = 0$. Then the output of N_1 will become 0 as $X_1 = 0$ and $\overline{Q} = 1$; while the output of N_2 will become 1 as $X_2 = 0$ and Q = 0. Thus one gets Q = 0 and $\overline{Q} = 1$.

However if one considers the initial states to be J = K = 0, Q = 1 and $\overline{Q} = 0$, then $X_1 = X_2 = 0$ which results in Q = 1 and $\overline{Q} = 0$. This indicates that the state of flip-flop outputs Q and $\overline{Q}$ remains unchanged for the case of J = K = 0.



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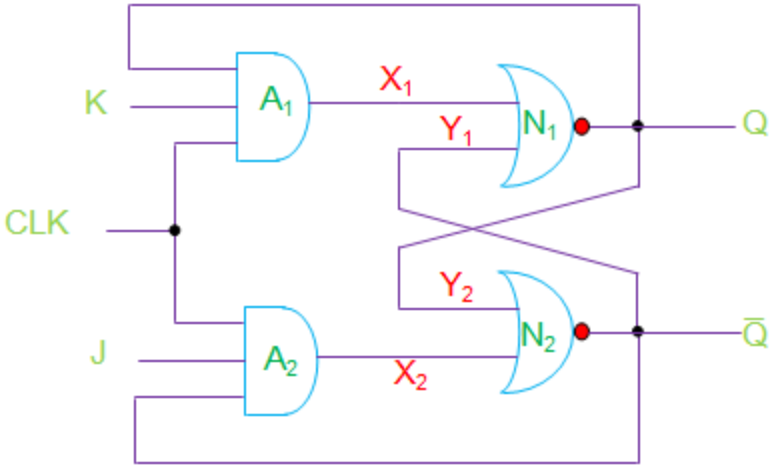
Now assume that J = 0, K = 1, Q = 0 and $\overline{Q}$ = 1. Analyzing on the same grounds, one gets $X_1 = X_2 = 0$ which further results in Q = 0 (and hence $\overline{Q}$ = 1). For the same case if Q and $\overline{Q}$ were 1 and 0, respectively, then $X_1 = 1$ and $X_2 = 0$ which would result in Q = 0 (and hence $\overline{Q}$ = 1). This implies that if J = 0 and K = 1, then the flip-flop resets (Q = 0 and $\overline{Q}$ = 1).

Next if J = 1, K = 0, Q = 1 and $\overline{Q}$ = 0, then $X_1 = X_2 = 0$ which results in Q = 1 (and thus $\overline{Q}$ = 0). For the same case if Q = 0 and $\overline{Q}$ = 1, then $X_1 = 0$, $X_2 = 1$ which leads to $\overline{Q}$ = 0 and hence Q is forced to value 1. This means that for the case of J = 1 and K = 0, flip-flop output will always be set i.e. Q = 1 and $\overline{Q}$ = 0.



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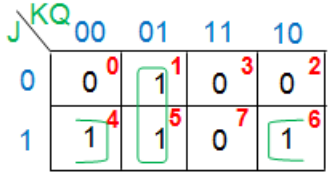
Similarly for J = 1, K = 1, Q = 1 and $\overline{Q}$ = 0 one gets $X_1 = 1$, $X_2 = 0$ and Q = 0 (and hence $\overline{Q}$ = 1); and if Q changes to 0 and $\overline{Q}$ to 1, then $X_1 = 0$, $X_2 = 1$ which forces $\overline{Q}$ to 0 and hence Q to 1. This indicates that for J = K = 1, flip-flop outputs toggle meaning which Q changes from 0 to 1 or from 1 to 0, and these changes are reflected at the output pin $\overline{Q}$ accordingly.

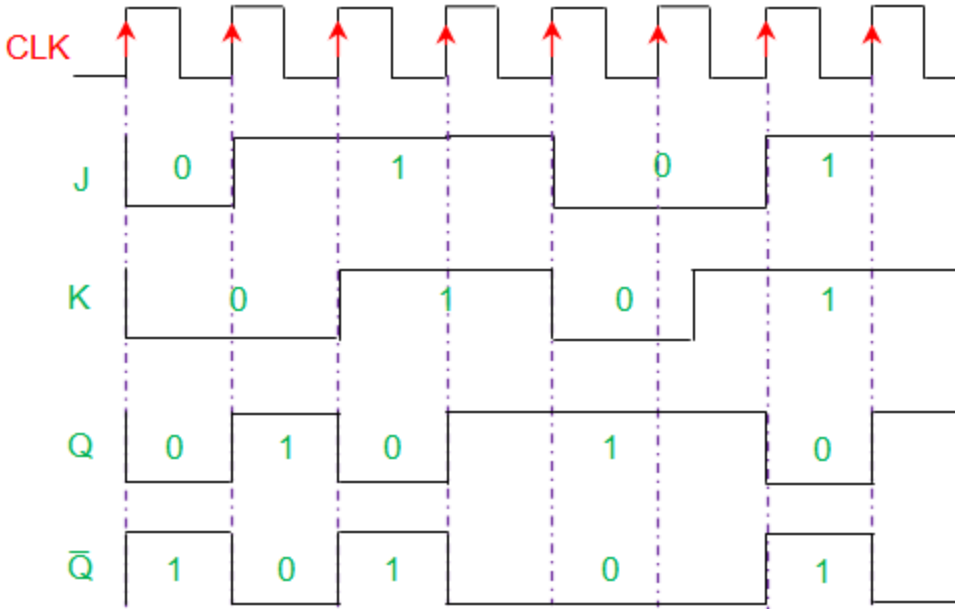
From the truth table one can arrive at the equation for the output of the J K flip-flop as **JQ' + K'Q** .



Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	$\overline{Q}$	Q	$\overline{Q}$	
↑	x	x	-		-		Latched
↑	0	0	0	1	0	1	No Change
↑			1	0	1	0	
↑	0	1	0	1	0	1	Reset
↑			1	0	0	1	
↑	1	0	0	1	1	0	Set
↑			1	0	1	0	
↑	1	1	0	1	1	0	Toggles
↑			1	0	0	1	

JK Flip Flop Timing Diagram

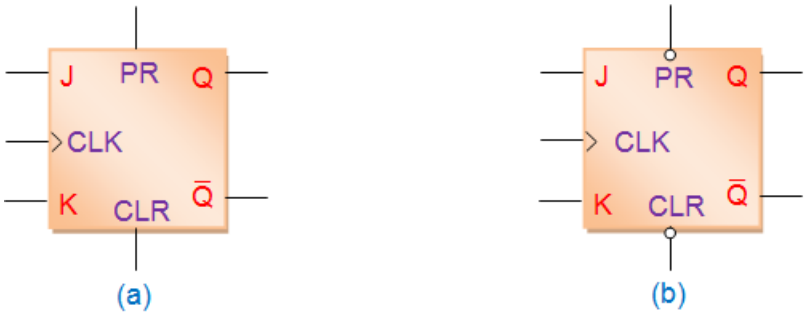
Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	$\bar{Q}$	Q	$\bar{Q}$	
✳	x	x	-		-		Latched
↑	0	0	0	1	0	1	No Change
↑			1	0	1	0	
↑	0	1	0	1	0	1	Reset
↑			1	0	0	1	
↑	1	0	0	1	1	0	Set
↑			1	0	1	0	
↑	1	1	0	1	1	0	Toggles
↑			1	0	0	1	



JK Flip Flop with CLR and PR

In addition to the basic input-output pins shown in previous Figure, **J K flip-flops** can also have special inputs like clear (CLR) and preset (PR). These can be used to bring the flip-flop to a definite state from its current state.

For example, the output can be made equal to 0 using CLR pin while it can set to 1 using PR pin. However these pins can be either active high (Figure a) or active low (Figure b) operated.



JK Flip Flop with CLR and PR

The waveforms pertaining to positive-edge triggered JK flip-flop with active high preset and clear pins are shown in Figure .

Moreover it is to be noted that these pins can be either synchronous or asynchronous in nature meaning which the clear and set operations occur either depending on the clock (shown by green lines) or no (shown by red lines), respectively.

Further if the preset and clear pins are active low, then the changes observed in the diagram occur at the instant when clear and preset go low instead of high.